Amendments to the Specification

Please amend the specification as follows:

Please replace the paragraph beginning on page 3, line 28 with the following amended paragraph:

As mentioned above, the present invention provides a liquid crystal display panel. The liquid crystal display panel comprises an upper substrate, a lower substrate, a liquid crystal layer, a common line layer, a gate line layer, an insulating layer, a passivation layer, a planar insulating layer, a data line layer, a plurality of thin film transistors, a plurality of transparent inter-digital pixel electrodes, and a plurality of transparent inter-digital counter electrodes. The lower substrate is parallel to the upper substrate and the liquid crystal layer is between the upper substrate and the lower substrate. The common line layer has a plurality of common lines on the lower substrate and the gate line layer also has a plurality of gate lines that are parallel to the common lines and formed on the lower substrate. The insulating layer is formed on the lower substrate, the common line layer, and the gate line layer. The data line layer has a plurality of data lines that are perpendicular to the gate lines and formed on the insulating layer. The plurality of thin film transistors are formed on the lower substrate, and each of the thin film transistors is positioned near a respective intersection portion of the gate lines and the data lines. The passivation layer is formed on the plurality of thin film transistors and the insulating layer. The planar insulating layer is formed on the passivation layer. The plurality of transparent inter-digital pixel electrodes is formed on the planar insulating layer. Each of the plurality of transparent inter-digital pixel electrodes has first fingers that extend in

the direction parallel to the data lines and are electrically connected to one corresponding drain of the thin film transistors through at least one first contact hole. The plurality of transparent inter-digital counter electrodes is formed on the planar insulating layer. ~~Each~~ One side of each of the plurality of transparent inter-digital pixel counter electrodes has second fingers that extend in the direction parallel to the data lines and is electrically connected to one corresponding common line through at least one second contact hole. In such case, a pixel region is defined by one of the data lines and one of the gate lines, the first contact hole and the second contact hole are on the same side of the pixel region, and the first fingers and the second fingers are interlaced in the pixel region.

Please replace the paragraph beginning on page 3, line 28 with the following amended paragraph:

As mentioned above, the present invention also provides a liquid crystal display panel. The liquid crystal display panel comprises an upper substrate, a lower substrate, a plurality of common lines, a plurality of gate lines, an insulating layer, a semiconductor layer, a plurality of sources, a plurality of drains, a passivation layer, a plurality of data lines, a plurality of transparent inter-digital pixel electrodes, and a plurality of transparent inter-digital counter electrodes. The lower substrate is parallel to the upper substrate and the liquid crystal layer is between the upper substrate and the lower substrate. The plurality of common lines and the plurality of gate lines are formed on the substrate and are parallel to each other. The insulating layer is formed on the substrate, the common lines, and the gate lines. The semiconductor layer is formed on the insulating layer and is above the gate lines. The plurality of sources and the plurality of drains are respectively formed on the two

sides of the semiconductor layer above one corresponding gate line. The passivation layer is formed on the space, the plurality of sources, the plurality of drains, and the insulating layer. The plurality of data lines is formed on the insulating layer, perpendicular to the plurality of gate lines, and electrically connected to one corresponding source. The plurality of transparent inter-digital pixel electrodes is formed on the passivation layer. Each of the transparent inter-digital pixel electrodes has first fingers that extend in the direction parallel to the data lines and is electrically connected to one corresponding drain through at least one first contact hole. The plurality of transparent inter-digital counter electrodes is formed on the passivation layer. ~~Each~~ One side of each of the transparent inter-digital pixel counter electrodes has second fingers that extend in the direction parallel to the data lines and are electrically connected to the corresponding common line through at least one second contact hole. A pixel region is defined by one of the data lines and one of the gate lines, the first contact hole and the second contact hole are on the same side of the pixel region, and the first fingers and the second fingers are interlaced in the pixel region.